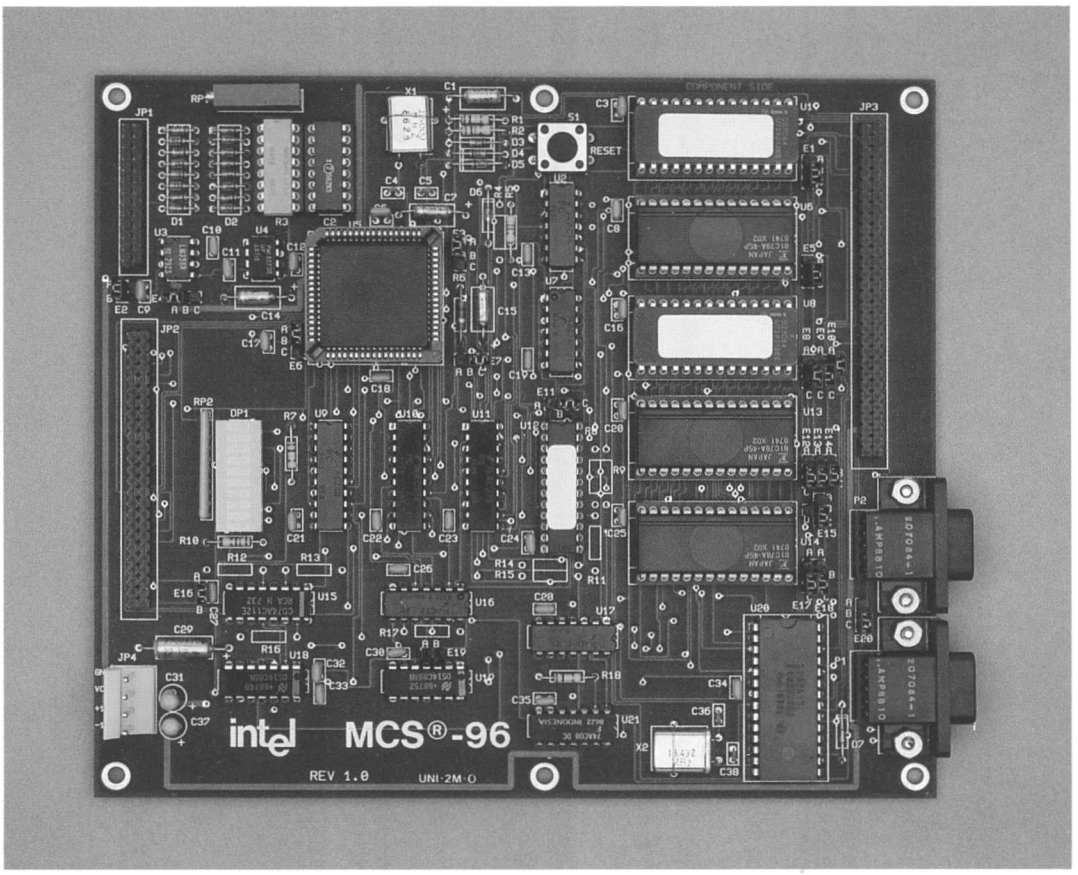
EV80C196KC EVALUATION BOARD



EV80C196KC FEATURES

- **Zero Wait-State 16 MHz Execution Speed**
- **24K Bytes of ROMsim**
- **Flexible Wait-State, Buswidth, Chip-Select Controller**
- **Totally CMOS, Low Power Board**
- **Concurrent Interrogation of Memory and Registers**
- **Sixteen Software Breakpoints**
- **Two Single Step Modes**
- **High-Level Language Support**
- **Symbolic Debug**
- **RS-232-C Communication Link**

LOW COST CODE EVALUATION TOOL

Intel's EV80C196KC evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 80C196KC advanced, CHMOS*, 16-bit microcontroller, the newest member of the industry standard MCS®-96 family. The board allows the user to take full advantage of the power of the MCS-96. The EV80C196KC provides zero wait-state, 16 MHz execution of a user's code. Plus, its memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

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APRIL 1989
Order number: 270802-001

Popular features such as a symbolic single line assembler/disassembler, single-step program execution, and sixteen software breakpoints are standard on the EV80C196KC. Intel provides a complete code development environment using assembler (ASM-96) as well as high-level languages such as Intel's iC-96 or PL/M-96 to accelerate development schedules.

The evaluation board is hosted on an IBM PC** or BIOS-compatible clone, already a standard development solution in most of today's engineering environments. The source code for the on-board monitor (written in ASM-96) is public domain. The program is about 1K, and can be easily modified to be included in the user's target hardware. In this way, the provided PC host software can be used throughout the development phase.

FULL SPEED EXECUTION

The EV80C196KC executes the user's code from on-board ROMsim at 16 MHz with zero wait-states. By changing crystals on the 80C196KC any slower execution speed can be evaluated. The boards host interface timing is not affected by this crystal change.

24K BYTES OF ROMSIM

The board comes with 24K bytes of SRAM to be used as ROMsim for the user's code and as data memory if needed. 16K bytes of this memory are configured as sixteen bits wide, and 8K bytes are configured as eight bits wide. The user can therefore evaluate the speed of the part executing from either buswidth.

FLEXIBLE MEMORY DECODING

By changing the Programable Logic Device (PLD) on the board, the memory on the board can be made to look like the memory system planned for the user's hardware application. The PLD controls the buswidth of the 80C196KC and the chip-select inputs on the board. It also controls the number of wait states (zero to three) generated by the 80C196KC during a memory cycle. These features can all be selected with 256 byte boundaries of resolution.

TOTALLY CMOS BOARD

The EV80C196KC board is built totally with CMOS components. Its power consumption is therefore very low, requiring 5 volts at only 300 mA. If the on board LED's are disabled, the current drops to only 165 mA. The board also requires +/- 12 volts at 15 mA.

CONCURRENT INTERROGATION OF MEMORY AND REGISTERS

The monitor for the EV80C196KC allows the user to read and modify internal registers and external memory while the user's code is running in the board.

SIXTEEN SOFTWARE BREAKPOINTS

There are sixteen breakpoints available which automatically substitute a TRAP instruction for a user's instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored in the ROMsim.

TWO STEP MODES

There are two single-step modes available. The first stepping mode locks out all interrupts which might occur during the step. The second mode enables interrupts, and treats subroutine calls and interrupt routines as one indivisible instruction.

HIGH LEVEL LANGUAGE SUPPORT

The host software for the EV80C196KC board is able to load absolute object code generated by ASM-96, iC-96, PL/M-96 or RL-96 all of which are available from Intel.

SYMBOLIC DEBUG

The host has a Single Line Assembler, and a Disassmbler, which recognize symbolics generated by Intel software tools.

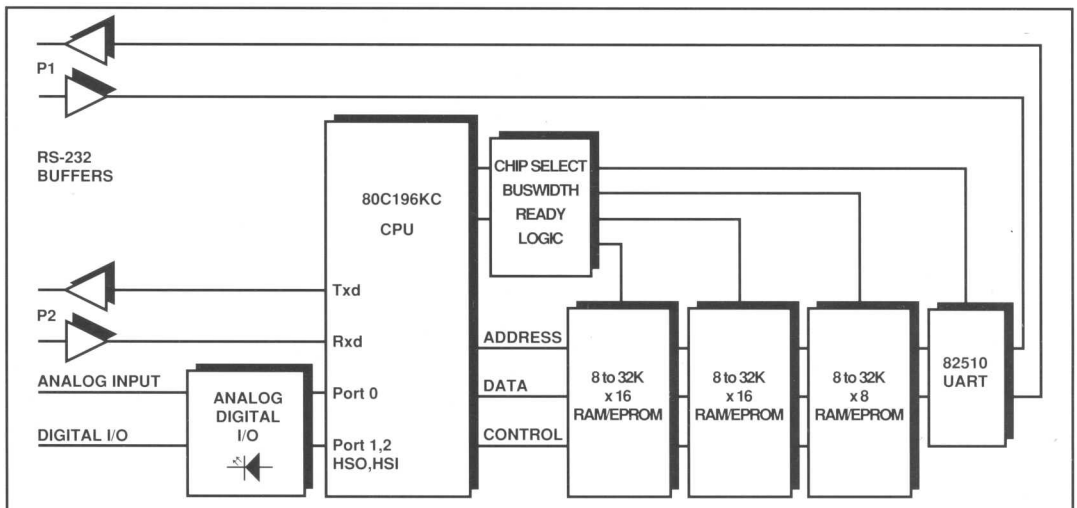
RS-232-C COMMUNICATION LINK

The EV80C196KC communicates with the host using an Intel 82510 UART provided on board. This frees the on-chip UART of the 80C196KC for the user's application.

PERSONAL COMPUTER REQUIREMENTS

The EV80C196KC Evaluation Board is hosted on an IBM PC, XT, AT** or BIOS compatible clone. The PC must meet the following minimum requirements:

- 512K Bytes of Memory
- One 360K Byte floppy Disk Drive
- PC DOS** 3.1 or Later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-96, iC-96 or PL/M-96
- A text editor such as AEDIT



Block Diagram of the 80C196KC Board